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METHOD AND APPARATUS FOR REDUCING ACIDIC CONTAMINATION ON A PROCESS WAFER FOLLOWING AN ETCHING PROCESS

FIELD OF THE INVENTION

001 This invention generally relates to shallow trench isolation (STI) etching apparatus and methods and more particularly to reducing acid contaminated residue associated therewith.

BACKGROUND OF THE INVENTION

002 In the integrated circuit industry today, hundreds of thousands of semiconductor devices are built on a single chip. Every device on the chip must be electrically isolated to ensure that it operates independently without interfering with another. The art of isolating semiconductor devices has become an important aspect of modern metal-oxide-semiconductor (MOS) and bipolar integrated circuit technology for the separation of different devices or different functional regions. With the high integration of the semiconductor devices, improper electrical isolation among devices will cause current leakage, and the

current leakage can consume a significant amount of power as well as compromise functionality. Among some examples of reduced functionality include latch-up, which can damage the circuit temporarily or permanently, noise margin degradation, voltage shift and cross-talk.

003 Shallow trench isolation (STI), is the preferred electrical isolation technique especially for a semiconductor chip with high integration. In general, conventional methods of producing an STI feature include forming a hard mask over the trench layer, patterning a photoresist etching mask over the hard mask, etching the hard mask through the photoresist etching mask to form a patterned hard mask, and thereafter etching the trench layer to form the STI feature. Subsequently, the photoresist etching mask is removed and the STI feature is back-filled with a dielectric material.

004 Frequently STI features are etched with a sequential process flow, where the mask layers are etched in one chamber and the silicon trench is etched in another chamber. Etching is

frequently performed by way of a plasma. Typically, in a plasma etching process an etchant source gas supplied to an etching chamber where the plasma is ignited to generate ions from the etchant source gas. Ions are then accelerated towards the process wafer substrate, frequently by a voltage bias, where they remove material (etch) from the process wafer. Various gas chemistries are used to provide variable etching rates for different etching target materials. Frequently used etchant sources include chloro and fluoro-hydrocarbons in addition to HBr to etch through for example, a silicon layer to form a shallow trench isolation feature. Another etchant chemistry, for etching through silicon, for example, includes a Cl_2 /O_2 /HBr-based chemistry. During and after the etching process halogen species such as chlorine and bromine remain on the target surface where, for example, they are incorporated into the sidewalls and bottoms of etched features as well as into overlying layers of photoresist. Since hydrogen is also present in and around the halogen species, highly corrosive acids may condense and form on the process wafer causing corrosive damage. HBr ,for instance,